IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:)
MATHIEU ET AL.)
)
Serial No. **Not yet assigned**)
)
Filing Date: **Herewith**)
)
For: **METHOD FOR THE PREPARATION AND EXECUTION OF A SELF-TEST PROCEDURE AND ASSOCIATED SELF-TEST GENERATING METHOD**)

I HEREBY CERTIFY THIS PAPER OR FEE IS BEING DEPOSITED WITH THE U.S. POSTAL SERVICE "EXPRESS MAIL POST OFFICE TO ADDRESSEE" SERVICE UNDER 37 CFR 1.10 ON THE DATE INDICATED BELOW AND IS ADDRESSED TO: BOX PATENT APPLICATIONS, ASSISTANT COMMISSIONER FOR PATENTS, WASHINGTON, D.C. 20231.

EXPRESS MAIL NO: EL769467732US
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NAME: Kyle Hopkinson
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PRELIMINARY AMENDMENT

Director, U.S. Patent and Trademark Office
Washington, D.C. 20231

Sir:

Prior to the calculation of fees and examination of the present application, please enter the amendments and remarks set out below.

In the Claims:

Please cancel Claims 1 to 11.

Please add new Claims 12 to 27.

12. A method for preparing and executing a self-test procedure to validate behavior of a processor model to be tested, the processor model being a processor or an associated simulator, the method comprising:

receiving specifications from a user including at least one instruction to be tested from among a set of instructions of the processor model;

reading, in a table, characteristic data of the processor model to be tested, the data comprising a functional definition of the at least one instruction to be tested and a functional definition of elements of the processor model;

executing the at least one instruction to be tested using the processor model;

computing an expected result following execution of the at least one instruction to be tested from the specifications from the user and the characteristic data of the processor model; and

causing the processor model to carry out a self-test procedure to validate the at least one instruction to be tested, the self-test procedure comprising initializing the elements of the processor model, executing the at least one instruction to be tested and obtaining a result, comparing the obtained result and the expected result, and returning a result word that is equal to a first value if the behavior of the processor model is right and a second value if the behavior of the processor model is not right.

13. The method according to Claim 12 wherein the at least one instruction to be tested comprises at least two instructions from the set of instructions of the processor model; and wherein the at least two instructions are executed successively to validate performance characteristics of the processor model.

14. The method according to Claim 12 further comprising:

determining if the result word is equal to the first value or the second value;

carrying out an additional self-test procedure if the result word is equal to the first value and if another self-test procedure has to be executed;

ending the method if the result word is equal to the first value and if another self-test procedure does not have to be executed; and

storing information for the self-test procedure if the result word is equal to the second value and ending the method, the information comprising an address at which an error has been detected.

15. The method according to Claim 14 further comprising initialization steps to be executed before causing the processor model to carry out the self-test procedure comprising:

receiving specifications from the user for at least two self-test procedures;

reading, in a table, characteristic data of the processor model necessary for the execution of the at least two self-test procedures; and

successively computing an expected result for each of the at least two self-test procedures.

16. The method according to Claim 15 further comprising, after successively computing an expected result for each of the at least two self-test procedures, providing a statistical study of the instructions to be tested during

subsequent steps to estimate a coverage of the set of instructions and performance characteristics of the processor model.

17. The method according to Claim 14 further comprising providing a statistical study at the end of the method of the result words returned during the self-test procedures executed by the processor model.

18. A method for generating self-test programs to validate behavior of a processor model to be tested, the processor model being a processor or an associated simulator, the method comprising:

receiving specifications from a user including at least one instruction to be tested from among a set of instructions of the processor model;

reading, in a table, characteristic data of the processor model to be tested, the data comprising a functional definition of the at least one instruction to be tested and a functional definition of elements of the processor model;

executing the at least one instruction to be tested using the processor model;

computing an expected result following execution of the at least one instruction to be tested from the specifications from the user and the characteristic data of the processor model; and

writing a self-test program to cause the execution of a self-test procedure by the processor model to validate the at least one instruction to be tested, the self-test procedure comprising initializing the elements of the processor model, executing the at least one instruction to be

tested and obtaining a result, comparing the obtained result and the expected result, and returning a result word that is equal to a first value if the behavior of the processor model is right and a second value if the behavior of the processor model is not right.

19. The method according to Claim 18 wherein the self-test program is written in an assembler type language.

20. The method according to Claim 18 wherein the self-test program is written in at least one of an advanced DGL and a C++ language.

21. The method according to Claim 18 wherein the at least one instruction to be tested comprises at least two instructions from the set of instructions of the processor model; and wherein the at least two instructions are executed successively to validate performance characteristics of the processor model.

22. The method according to Claim 18 further comprising:

determining if the result word is equal to the first value or the second value;

carrying out an additional self-test procedure if the result word is equal to the first value and if another self-test procedure has to be executed;

ending the method if the result word is equal to the first value and if another self-test procedure does not have to be executed; and

storing information for the self-test procedure if the result word is equal to the second value and ending the method, the information comprising an address at which an error has been detected.

23. The method according to Claim 18 wherein initializing the elements of the processor model is performed based upon instructions from the set of the instructions of the processor model.

24. A device for executing a self-test procedure on a processor model to validate behavior thereof, the processor model being a processor or an associated simulator, the device comprising:

a central processing unit for

receiving specifications from a user including at least one instruction to be tested from among a set of instructions of the processor model,

reading, in a table, characteristic data of the processor model to be tested, the data comprising a functional definition of the at least one instruction to be tested and a functional definition of elements of the processor model,

causing the processor model to execute the at least one instruction to be tested,

computing an expected result following execution of the at least one instruction to be tested from the specifications from the user and the characteristic data of the processor model, and

causing the processor model to carry out a self-test procedure to validate the at least one

instruction to be tested, the self-test procedure comprising initializing the elements of the processor model, executing the at least one instruction to be tested and obtaining a result, comparing the obtained result and the expected result, and returning a result word that is equal to a first value if the behavior of the processor model is right and a second value if the behavior of the processor model is not right.

25. The device according to Claim 24 wherein the at least one instruction to be tested comprises at least two instructions from the set of instructions of the processor model; and wherein the at least two instructions are executed successively to validate performance characteristics of the processor model.

26. The device according to Claim 24 wherein said central processing unit further determines if the result word is equal to the first value or the second value, carries out an additional self-test procedure if the result word is equal to the first value and if another self-test procedure has to be executed, ends the self-test procedure if the result word is equal to the first value and if another self-test procedure does not have to be executed, and stores information for the self-test procedure if the result word is equal to the second value and ends the method, the information comprising an address at which an error has been detected.

27. The device according to Claim 26 wherein said central processing unit initializes the processor model before

causing the processor model to carry out the self-test procedure by receiving specifications from the user for at least two self-test procedures, reading characteristic data in a table of the processor model necessary for the execution of the at least two self-test procedures, and successively computing an expected result for each of the at least two self-test procedures.

REMARKS

It is believed that all of the claims are patentable over the prior art. For better readability and the Examiner's convenience, the newly submitted claims differ from the translated counterpart claims which are being canceled. The newly submitted claims do not represent changes or amendments that narrow the claim scope for any reason related to the statutory requirements for patentability.

Accordingly, after the Examiner completes a thorough examination and finds the claims patentable, a Notice of Allowance is respectfully requested in due course. Should the Examiner determine any minor informalities that need to be addressed, he is encouraged to contact the undersigned attorney at the telephone number below.

In re Patent Application of:
MATHIEU ET AL.
Serial No. **Not yet assigned**
Filing Date: **Herewith**

Respectfully submitted,

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